214400US-2



IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF :

YASUO YAMAGUCHI : EXAMINER: CRUZ, L. C.

SERIAL NO: 09/964,462 :

FILED: SEPTEMBER 28, 2001 : GROUP ART UNIT: 2827

FOR: SEMICONDUCTOR DEVICE :



AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Responsive to the Official Action mailed June 25, 2002, please amend the above-identified patent application as follows:

IN THE SPECIFICATION

Page 25, please replace the paragraph at lines 13-21 as follows:

In a semiconductor device 104 shown in Fig. 7, an insulation film 30 is formed in place of the n-type semiconductor layers 3, 13 in the substrate 1. The insulation film 30 is selectively formed in the positions directly under the contact holes into which the plugs 9, 19 are filled on the principal plane of the substrate 1. Therefore, the insulation film 30 is interposed between the plugs 9, 19 and the semiconductor layer 2. The insulation film 30 can be readily formed as an oxide film by selectively oxidizing the principal plane of the substrate

1 via contact holes after the contact holes into which the plugs 9, 19 are to be filled have been formed in the insulation layer 4,6.

IN THE CLAIMS

1. (Amended) A semiconductor device comprising:

a substrate having a principal plane;

an insulation layer formed on said principal plane;

a heat generating layer embedded in said insulation layer and opposing to said principal plane with a part of said insulation layer interposed between the heat generating layer and the substrate;

a first wiring layer disposed on said insulation layer;

a second wiring layer disposed on said insulation layer;

a first plug embedded in said insulation layer, a lower end of the first plug being connected to one end of said heat generating layer and an upper end of the first plug being connected to said first wiring layer, said first plug having a rectangular cross sectional shape along said principal plane of which short sides are parallel to a main direction connecting said one end and the other end of said heat generating layer and long sides are parallel to a direction perpendicular to said main direction;

a second plug embedded in said insulation layer, a lower end of the second plug being connected to said other end of said heat generating layer and an upper end of the second plug connected to said second wiring layer; and

a third plug embedded in said insulation layer, an upper end of the third plug being connected to said first wiring layer or said first plug and a lower end of the third plug reaching said principal plane, wherein each of the first, second and third plugs is conductive.

10. (Amended) The semiconductor device according to claim 1, further comprising a fourth plug embedded in said insulation layer, of which upper end is connected to said second wiring layer or said second plug and lower end reaches said principal plane, wherein the fourth plug is conductive.

11. (Amended) A semiconductor device comprising:

a substrate having a principal plane;

an insulation layer formed on said principal plane and made of a low dielectric constant insulator;

a heat generating layer embedded in said insulation layer and opposing to said principal plane with a part of said insulation layer interposed between the heat generating layer and the substrate;

a first wiring layer disposed on said insulation layer;

a second wiring layer disposed on said insulation layer;

a first plug embedded in said insulation layer, a lower end of the first plug being connected to one end of said heat generating layer and an upper end of the first plug being connected to said first wiring layer;

a second plug embedded in said insulation layer, a lower end of the second plug being connected to an other end of said heat generating layer and an upper end of the second plug being connected to said second wiring layer; and

a third plug embedded in said insulation layer, an upper end of the third plug being connected to said first wiring layer or said first plug and a lower end of the third plug reaching said principal plane, wherein each of the first, second and third plugs is conductive.

15. (Amended) The semiconductor device according to claim 11, wherein said first wiring layer is a wiring layer for transmitting stable potential, a width of the first wiring layer being elongated so as to be larger than or equal to a width based on a design rule in a region including a connection portion between said first wiring layer and said first plug.

17. (Amended) The semiconductor device according to claim 11, further comprising a fourth plug embedded in said insulation layer, an upper end of the fourth plug being connected to said second wiring layer or said second plug and a lower end of the fourth plug reaching [reaches] said principal plane, wherein the fourth plug is conductive.

18. (Amended) A semiconductor device comprising:

a semiconductor substrate having a principal plane;

an insulation layer formed on said principal plane;

a heat generating layer embedded in said insulation layer and opposing to said principal plane with a part of said insulation layer interposed between the heat generating layer and the semiconductor substrate;

a first wiring layer disposed on said insulation layer;

a second wiring layer disposed on said insulation layer;

a first plug embedded in said insulation layer, a lower end of the first plug being connected to one end of said heat generating layer and an upper end of the first plug being connected to said first wiring layer;

a second plug embedded in said insulation layer, a lower end of the second plug being connected to an other end of said heat generating layer and an upper end of the second plug being connected to said second wiring layer; and

a third plug embedded in said insulation layer, an upper end of the third plug being connected to said first wiring layer or said first plug and a lower end of the third plug reaching said principal plane, the third plug forming a Schottky barrier between the third plug and said semiconductor substrate, wherein each of the first, second and third plugs is conductive.

## REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

In the outstanding Official Action, the drawings were objected to; the disclosure was objected to for minor informalities; Claims 1-20 were rejected under 35 U.S.C. § 112, second paragraph; Claims 1-5 and 9-20 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,779,127 to Honjo; and Claims 6, 7 and 8 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Honjo.

Claims 1-20 are presently active in this case, Claims 1, 11 and 18 are amended by way of the present amendment.

First, Applicant wishes to thank Examiner Cruz for the July 31, 2002 telephone interview at which time the outstanding issues in this case were discussed. During the discussion, Applicant presented arguments and amendments substantially as indicated in this response. While no agreement was reached, Examiner Cruz indicated that she would give careful consideration to the presented amendment and arguments when filed in a formal response.

With regard to the objection to the drawings, Applicant traverses this objection. Figure 2 is objected to as showing a Reference number 4 that is not described in the

specification. However, Figure 2 includes no Reference designation 4. Therefore, Applicants read the objection as an objection to Figure 21, which does include a reference designation 4. Submitted herewith is a separate Letter Requesting Approval of Drawing Changes, which changes remove the reference numeral 4 from Figure 21. Upon receiving approval of the requested drawing changes, Applicants will submit formal drawings incorporating the changes.

With regard go the objection to the disclosure, Applicant has now amended the specification to correct the noted informalities. Therefore, the objection to the disclosure is believed to be overcome.

With regard to the rejection under 35 U.S.C. § 112, second paragraph, Claims 1, 11, 15, 17 and 18 have been amended to correct the noted and discovered informalities, and therefore the rejection under 35 U.S.C. § 112, second paragraph, is believed to be overcome. If, however, the Examiner disagrees, the Examiner is invited to telephone the undersigned who will be happy to work with the Examiner in a joint effort to derive mutually satisfactory claim language.

Turning now to the merits, in order to expedite issuance of a patent in this case, Applicant has amended Claims 1, 11 and 18 to clarify the patentable features of the invention over the cited reference to Honjo. Specifically, Applicant's Claims 1, 11, and 18 recite a semiconductor device including a substrate having a principal plane, an insulating layer formed on the principal plane and a heat generating layer embedded in the insulation layer and opposing the principal plane with a part of the insulation layer interposed between the heat generating layer and the substrate and first and second wiring layers disposed on the insulation layer. Also recited is a first plug embedded in the insulation layer, a lower end of the first plug being connected to one end of the heat generating layer and an upper end of the

first plug being connected to the first wiring layer, a second plug embedded in the insulation layer, a lower end of the second plug being connected to another end of the heat generating layer and an upper end of the second plug being connected to the second wiring layer, and a third plug embedded in the insulation layer, an upper end of the third plug being connected to the first wiring layer or the first plug and a lower end of the third plug reaching the principal plane.

In contrast, the reference to Honjo discloses a three dimensional integrated circuit having minimum interconnections. As seen in Figure 3 of Honjo, the integrated circuit includes a multilayer structure 31 having several regions. As discussed in the telephone interview, the outstanding Official Action cites item 34 in Figure 3 of Honjo as the heat generating layer, item 32 as the substrate, and item 40 as the first wiring layer. In this regard, Applicant first notes that item 34 is not embedded in an insulation layer with a part of the insulation layer interposed between the heat generating layer 34 and the substrate 32 as required in Applicant's Claims 1, 11 and 18. More specifically, the substrate 32 of Honjo has a P-doped semiconductor region 33 on top of the substrate without any insulation layer. Moreover, while the Official Action cites item 45 in Honjo's Figure 3 as the third plug, this region of the integrated circuit does not reach the principal plane of the substrate 32. Thus, Claims 1, 11 and 18 patentably define over Honjo.

Regarding claims 1 and 14, one of the features of those claims resides in that the first plug has a specific rectangular cross sectional shape. The advantages of the recited feature, i.e., the rectangular cross section shape of the first plug having short sides and long sides which are arranged in respective predetermined (as specified in the claims) directions, are described in the specification on page 19, line 18 through page 20, line 4.

Regarding claim 11, it is general that a given substance must have a dielectric constant on the order of 10°, in order to be usable as a material for a low dielectric constant film. SiOC which is exemplarily cited in the present specification, for example, can be used as a material for a low dielectric constant film because the dielectric constant thereof is about 2.8. In contrast, a depletion layer 14 of Honjo is formed of GaAs, and an undoped GaAs semiconductor layer 35 is formed of GaAs. It should be noted that the dielectric constant of GaAs is approximately $10^1$, so that neither the depletion layer 14 nor the undoped GaAs semiconductor layer 35 can be recognized as a low dielectric constant film in light of the knowledge of one having ordinary skill in the art. Accordingly, the depletion layer 14 of Honjo does not correspond to the recited low dielectric constant insulator of the present claim 11.

Regarding claim 18, a dope region 45 of Honjo is a $p^+$-type semiconductor. Hence, in Honjo, a Schottky barrier does not occur between the dope region 45 and a p-type GaAs semiconductor layer 33 which corresponds to the recited principal plane of the semicondutor substrate.

Regarding claims 3 and 13, the p-type GaAs semiconductor layer 33 of Honjo is considered to correspond to the recited first semiconductor layer. Thus, it is clear that Honjo does not disclose any element corresponding to the recited second semiconductor layer which is formed to be surrounded by the first semiconductor layer ("the p-type GaAs semiconductor layer 33" in Honjo).

Regarding claims 5 and 15, it is clear that Honjo does not disclose or suggest that a stable potential is provided to a metal layer 40 (corresponding to the recited first wiring layer) event by making reference to Fig. 4 of Honjo, which is confirmed by lines 3-7 of column 6 of Honjo, for example.

Regarding claims 6 and 8, those claims specify the product of the lengths L and S, which produces unexpected results as described in the present specification on page 21, lines 2-11.

Regarding claims 10 and 17, an isolation region 37 of Honjo does not correspond to a conductive plug.

Therefore, Applicant's Claims 1, 11 and 18 patentably define over the cited reference to Honjo. Moreover, as Claims 2-10, 12-17, and 19-20 depend from Claims 1, 11 and 18 respectively, these claims also patentably define over the cited reference.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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